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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,321	03/21/2001	Gary F. Feierbach	ALP1P203	4455

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	4

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/814,321	FEIERBACH, GARY F.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 21, 2001 was filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 8, 17, 19, 26, and 33 are objected to because of the following informalities:

- as per claim 8, the phrase "said operations" on line 5 does not have corresponding antecedent and should be corrected to "the steps".
- as per claims 17 and 26, the independent claims are almost identical except for the phrase "said functional unit to be individually" on line 27 of claim 26. The distinction is not readily apparent in significance and thus, the overall number of claims may have been reduced by eliminating one set of the associated claim. In general, the Office will still examine the claims in their own merits.
- as per claim 19, the word/phrase "receivingcurrent" on line 25 should be corrected to "receiving current".
- as per claim 33, the referenced "claim 1" on line 18 appears to be erroneous. The Office will assume the referenced independent claim to be 26 for examination.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley, U.S. Patent 6219796, in view of Fletcher et al., U.S. Patent 6611920, hereinafter referred to as Fletcher.

5. As per claims 1, 9, 17, 21-23, 26, 32-34, and 37, Bartley taught power management of multiple-functional-units processors comprising of:

- an instruction evaluation unit that evaluates a next instruction to be executed and produces activity indicators[1] [FIG. 1; column 4, lines 54-57; column 5, lines 1-2, 33-44, 51-57]; and
- each of plurality of functional units independently controllable by the instruction type [column 3, lines 1-15; column 5, lines 1-50].

6. However, Bartley did not expressly disclose managing power at a more "fine-grained" level within the functional units and further conserve power consumption.

7. Fletcher taught a power control system for an integrated circuit comprising of:

- a functional unit with a plurality of stages for executing instructions [FIG. 3, item 310; column 4, line 6-7];
- a stage activation controller that utilizes the activity indicators to activate or deactivate the respective stages [FIG. 3, items 340.x and VALID]; and

- each of plurality of stages capable of being separately activated or deactivated individually based upon a respective activity indicator [column 2, lines 45-48; column 4, lines 12-14].

8. An ordinary artisan at the same time the invention was made would have been motivated to look for an optimal way to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [see Fletcher: column 1, lines 13-32].

9. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Bartley and Fletcher to provide a power management system based on activity indicators of instructions for processors with a plurality of functional units comprising of a plurality of stages.

10. As per claims 1 and 9, Fletcher taught advancing instructions and executing instructions within each of selected stages [column 4, line 61 to column 5, line 5].

11. As per claims 2, 10, 14, 18, 28, 35, and 38, Bartley taught a very long instruction word processor [column 3, lines 41-44].

12. As per claim 3, Bartley taught evaluating whether instruction type is no-operation or operation [column 4, lines 54-57].

13. As per claims 4, 9, and 19, Fletcher taught the type of instructions executed in each of selected stages is an instruction type[2] [column 4, lines 27-60].

14. As per claims 5 and 6, Bartley taught producing power-on activity indicators associated with operation instructions and power-off activity indicators associated with no-operation instructions [column 4, lines 56-57; column 5, lines 51-54; column 6, lines 8-11].

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[1] The instructions are converted to appropriate machine codes indicating whether an instruction is "active" or not.

15. As per claims 7, 11, and 30, Fletcher taught transmitting a clock signal only to the selected stages of the functional unit [FIG. 3, item 342; column 4, lines 10-14].

16. As per claims 8 and 16, Bartley taught repeating steps for all instructions [FIG. 7].

17. As per claims 9 and 11, Fletcher taught transmitting a null-bit when the instruction is no-operation and a 1-bit when the instruction is an operation [column 4, lines 30-33, 48-52].

18. As per claims 12, 25, 27, and 29, Fletcher taught transmitting a clock signal to the memory device, the clock signal to each of the stages being transmitted after the signal to the memory device is transmitted [FIG. 3, items 342 and 340.x; column 4, lines 6-47].

19. As per claims 13, 15, 22-24, 33-34, and 36, Fletcher taught a plurality of functional units with each functional unit connected to a respective one of plurality of memory devices [FIG. 3, items 340.x; column 2, lines 25-34].

20. As per claims 20-21, 23, 31-32, and 34, Fletcher taught the stage activation controller as a memory unit to store activity indicators [FIG. 3, items 340.x].

21. As per claim 27, instruction registers containing next operation to be executed are well known in the art of pipeline processing [see Bartley: FIG. 2].

22. As per claim 37, an ordinary artisan would be motivated to incorporate the power-saving processor with a computer system [see Fletcher: FIG. 1] comprising of elements well known in the art:

- a main memory for storing data, including instructions;
- I/O devices; and
- at least one bus interconnecting components of the system.

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[2] The valid/activity-indicator signal will be activated only for active instructions; thus, no-operation type instructions

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Yamada, U.S. Patent 5495617, disclosed power management system to determine which portion of functional unit should be enabled based on instruction to be executed.

b. Jackson, U.S. Patent 5825674, disclosed a power management system utilizing no-operation type instructions.

c. Matter, U.S. Patent 5392437, disclosed a method for powering-up and powering-down functional units.

d. Minematsu, U.S. Patent 6550000, disclosed a processor capable of executing instructions in parallel with multiple functional units.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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won't execute and draw power at respective stages as the clock signal is disabled.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
February 6, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100